Listing of the Claims

1. - 27. (Cancelled)

28. (Original) A semiconductor structure of a damascene or dual damascene interconnect formed by a trench-filling process of electroplated Cu having an as-deposited grain size of not less than 0.5 μm and a decrease in electrical resistance of at least 15% after a time period of not more than 30 hours at about 21°C.

29. (Currently amended) A semiconductor structure of a damascene or dual damascene interconnect according to claim 28, wherein said as-deposited grain size of electroplated Cu is between about 0.5 μm and about [[.15]] 1.5 μm.

30. (Original) A semiconductor structure of a damascene or dual damascene interconnect according to claim 28, wherein said grain size of said electroplated Cu after said time period of not more than 30 hours at about 21°C is between about 1.5 μm and about 2 μm.